T.O. 12S5-4-19-2

TECHNICAL MANUAL

FIELD MAINTENANCE

TTY ADAPTER

399R-1

(COLLINS)

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Type of Service (optional combinations of the following are possible)	a. Full-Duplex or Half-Duplex Operation b. 5 ma or 60 ma transmit/receive loop c. 60 wpm or 100 wpm transmit/receive speed
Number of Channels	Single Channel
Form Factor	1/4 ATR long
Dimensions	2-1/4 x 7-5/8 x 19 inches
Weight	14 pounds maximum
Type of Construction	Plug-in printed circuit boards and modules on an aluminum chassis
Audible Noise	None
Number of Units	One
Operational Temperature Range	-20°C to +55°C
Survival Temperature Range	-62°C to +70°C
Operational Humidity Range	0 to 100 percent
Operation Altitude Range	Sea Level to 50,000 feet
Explosion	The equipment will not cause ignition of an ambient-explosive-gaseous mixture with air when operating in such an atmosphere

Figure 1-2. Table of Equipment Characteristics

CARD NAME	Quantity Required	TRANSISTORS (Per Card)									DIODES (Per Card)								
		2N43A	2N404	2N526	2N495	2N657	2N697	2N333	2N718	2N1212	1N663	1N758A	1N755A	1N750A	1N645	1N753A	1N547	1N1124A	691980
TOX 3 (A1)	1	1									1								
TOX 2 (A2)	1		1	2							2	1							
TOX 1 (A3)	1		2								3								
FLIP-FLOP (A4, A6, A7, A8, A24, A25, A27)	7		4								12								
LOGIC 1 (A5, A26)	2										8								
LOGIC 2 (A9)	1										10		1						
INVERTER B (A10)	1										6								
LOGIC 3 (A11)	1										10		1						
KEYER (A12)	1					3	1								1				
RESISTOR 2 (A13)	1																		
RESISTOR 1 (A14)	1																		
POWER SUPPLY REGULATOR (A15, A16)	2				1	1	1							1	1	2			
POWER SUPPLY CAPACITORS (A17, A18)	2																		
SWITCH (A19)	1																		
4KC OSCILLATOR A (A20)	1							1											
4KC OSCILLATOR B (A21)	1							1											
INVERTER A (A22, A28)	2		6								6								
120 VOLT POWER SUPPLY (A23)	1																4		
STRAP (A29)	1																		
TEST POINTS (A30)	1																		
5MA LOOP CONTROL (A31)	1		1	1			1		1		11				1				
HEAT SINK (A35)	1									2								4	2

Figure 1-3. Circuit Card and Semiconductor Complement

SECTION II

PREPARATION FOR USE AND RESHIPMENT

2-1. UNPACKING AND INSPECTION.

2-2. Open the packing case, and remove all packing material. Take care not to damage the equipment shipping container or internal packing material. Carefully remove the equipment from the packing case. Store the packing case and packing material in a clean, dry place until required for reshipment, storage, or inspection by the transportation company (in case of a damage claim). Inspect the equipment for damage. Notify the transportation company immediately if the 399R-1 Teletype Adapter is damaged on receipt.

2-3. INSTALLATION.

2-4. Installation instructions for the 399R-1 Teletype Adapter depend upon the particular system arrangement in which the adapter is to be integrated. If it is to be used in conjunction with other adapter equipments, it should be installed in an arrangement that provides maximum efficiency for the operator. If installed separately, the adapter should be mounted in a 1/4 ATR long vibration tray. The mounting tray must have an integral rear-mounted 32-pin connector which mates with the 32-pin connector on the rear of the 1/4 ATR long case. The 399R-1 requires a 115 volt ac, 400 cps single phase power source. It is housed in a non-pressurized case and is cooled by radiation and convection. Before installing the 399R-1 Teletype Adapter, it is necessary to check the position of the switch on card A19. If the 399R-1 power supply is to be used for other equipment, the switch should be set to the EXT position. If the 399R-1 is to be operative itself, the switch is set to the 399R-1 position.

2-5. Install Teletype Adapter 399R-1 as follows:

a. Ensure that the KEY LINE and PWR switches (figure 2-1) are positioned at OFF.

b. Turn the fastener thumbscrew counterclockwise as far as it will go.

c. Insert the 399R-1. Push toward the rear until the rear connector is fully engaged. Do not force. Hold in place.

d. Place the cup washer and thumbscrew over the receiver mounting lug. Turn the thumbscrew clockwise as far as it will go. Do not force.

e. Safety-wire the thumbscrew in place.

2-6. INITIAL TURN-ON.

2-7. The following steps are necessary for initial turn-on:

a. With a screwdriver, set the KEYER INPUT control to the MARK position.

b. With a screwdriver, position the REC LOOP ADJ and XMT LOOP ADJ controls fully counterclockwise.

c. Set the PWR and KEY LINE switches to ON.

d. Plug a milliammeter into the XMT LOOP TEST phone jack.

Figure 2-1. 399R-1 Operating Controls

g. Turn the RCV LOOP ADJ control clockwise until a 60 ma deflection is noted on the milliammeter.

h. Set the KEYER INPUT control to the RCV DATA position.

2-8. PREPARATION FOR STORAGE AND RESHIPMENT.

2-9. Repack and store the 399R-1 Teletype Adapter in the original package. Use the air cell padding originally supplied. Obtain the necessary bags of desiccant, and package with the 399R-1 inside the vapor barrier bag. An airtight polyethylene bag may be used instead of the original vapor barrier bag, if necessary. It should be carefully sealed.

2-10. Equipment to be reshipped should be packaged in the original shipping cartons. Internal packaging, fillers, and blocking should be replaced in the same manner as in the original shipment.

SECTION IV

THEORY OF OPERATION

4-1. GENERAL. Provisions are made for optional selection of either a 5 ma or 60 ma teletype loop, as well as either full-duplex or half-duplex operation (figure 4-1). In the receive function, the 399R-1 Teletype Adapter accepts binary data in Baudot code which keys a loop circuit to operate a teletype printer, tape punch, or a storage unit at 60 or 100 wpm. In the transmit function, the 399R-1 Teletype Adapter accepts single channel 60 or 100-wpm serial nonsynchronous Baudot-coded data from a teletype keyboard, tape reader, or storage unit. It synchronizes the accepted data with internal timing for subsequent transmission to a receiving station or stations. The conversion from nonsynchronous to synchronized data is performed in a shift (storage) register. The required transmit timing is derived from an external source.

4-2. RECEIVE OPERATION.

4-3. During the receiving operation (figure 4-2), in both full-duplex and half-duplex, the 399R-1 Teletype Adapter accepts 60 or 100-wpm Baudot-coded binary data from an external source. During half-duplex operation a squelch or inhibit signal is applied to the TOX circuit so that no transmit signals can be sent to transmitting equipment. The accepted data bits are fed through single or double inversion circuits as necessary to achieve a correct signal format. From the inversion circuitry the data is applied through a control gate. The control gate either enables or inhibits the flow of received data to the keyer circuitry. This permits unit selection when two or more 399R-1 units are used. The keyer circuit functions as a transistorized switch. Each mark bit applies forward bias to the base of the switching transistor, thereby triggering the teletype loop to operate a teletype printer, tape punch, or storage unit.

4-4. TRANSMIT OPERATION.

4-5. Full-duplex transmit operation is accomplished in two functional areas (figure 4-3). These are the transmit-loop and the speed normalizer circuits. These circuits are discussed separately.

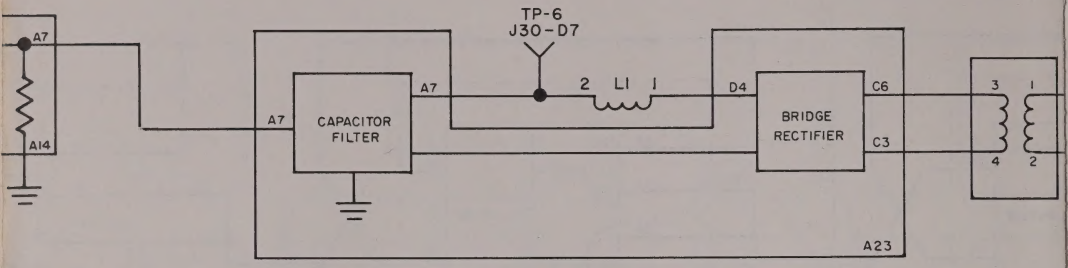
4-6. TRANSMIT LOOP. During the full-duplex transmit operation, 100-wpm Baudot-coded data is accepted from a keyboard, tape reader, or storage unit. In the 60 ma loop the data bits are adjusted for proper current rating and then fed into a resistance network to achieve proper levels for processing in the speed normalizer circuitry. In the 5 ma loop, the data is fed through a transistorized loop switch. This loop switch provides a method of unit selection, where two or more units are used. The output of the 60 ma loop resistance network or the 5 ma loop switch, as selected, is fed into the speed normalizer circuitry for signal synchronizing.

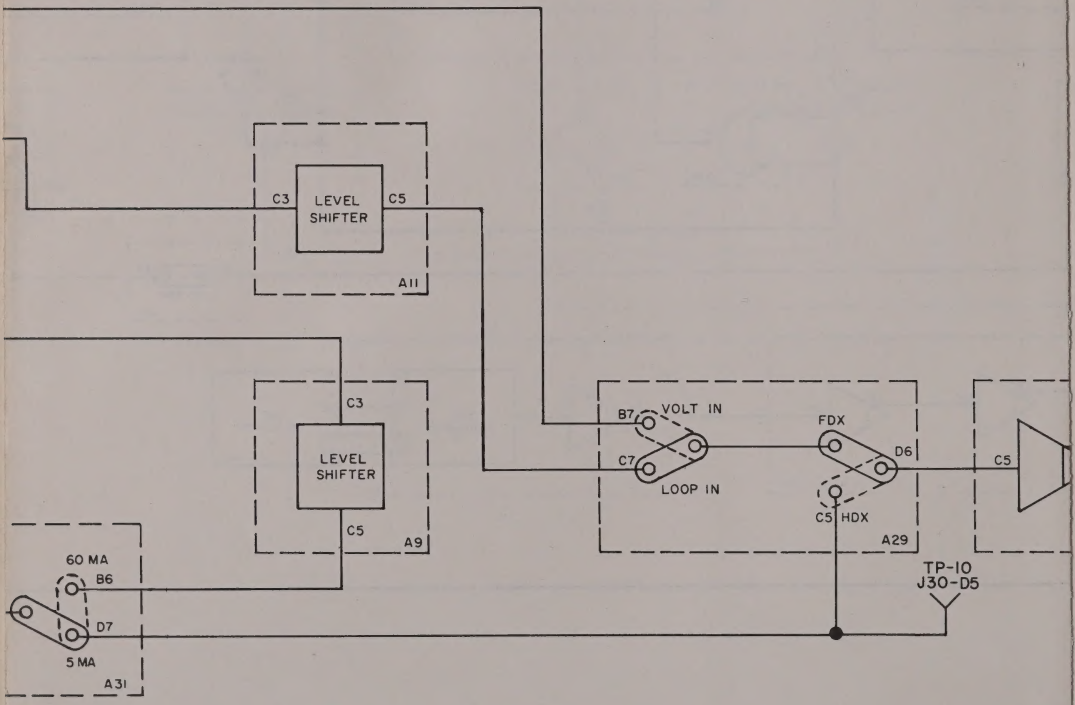
4-7. In half-duplex operation, the data to be transmitted is fed through the selected-loop keyer circuit (described in paragraph 4-3). There are two outputs from the keyer. One is fed to the teletype printer, in receive function. The other output of the keyer circuit is applied to the speed normalizer circuitry.

4-8. SPEED NORMALIZER. In full-duplex operation the transmit data is fed through data level-shifting circuitry to achieve signal voltage levels which are compatible to the speed normalizer circuitry. In half-duplex operation this is necessary only if the 60 ma loop is chosen. The data to be transmitted is fed through inversion circuitry to achieve correct signal format. Data from the inversion circuitry is applied to a shift register. This register, with its associated counter circuitry, synchronizes the transmit data so that all bits are of equal time duration. A bit counter circuit advances data into the first stage of the register. A sample timing circuit advances the data from the first to the second register stage. Data advances from the second to the third register stage in synchronism with the 75 cps external timing signal. The output of the third register stage is inverted for correct format and is transferred to external equipment for transmission.

4-9. TOX (TELETYPE-OPERATE-TRANSMIT) CIRCUIT.

4-10. A teletype-operate-transmit circuit is incorporated in the 399R-1 Teletype Adapter. The circuit is a teletype net-in-use monitor and automatic keying device. A space or start bit in the teletype transmit data will cause the TOX circuit to actuate the transmit keyline relay, thereby closing the transmit keyline. A delay circuit is incorporated to prevent release of the keyline relay for 6 seconds so that subsequent data or momentary line interruptions will not open the keyline. If the net is already in use, a squelch signal from external equipment will prevent seizure of the transmit line. Operation of the keyline relay, in addition to closing the keyline, supplies a level to place external transmission equipment in transmit mode. An external ground may be applied to lock the keyline relay in the actuated state thereby overriding previous conditions.


A7
A14
A7
CAPACITOR FILTER
A7
TP-6
J30-D7
2
L1
1
D4
BRIDGE RECTIFIER
C6
C3
3
1
4
2
A23


C3
LEVEL SHIFTER
C5
A11
C3
LEVEL SHIFTER
C5
A9
B7
VOLT IN
C7
LOOP IN
FDX
D6
C5 HDX
A29
C5
60 MA
B6
D7
5 MA
A31
TP-10
J30-D5

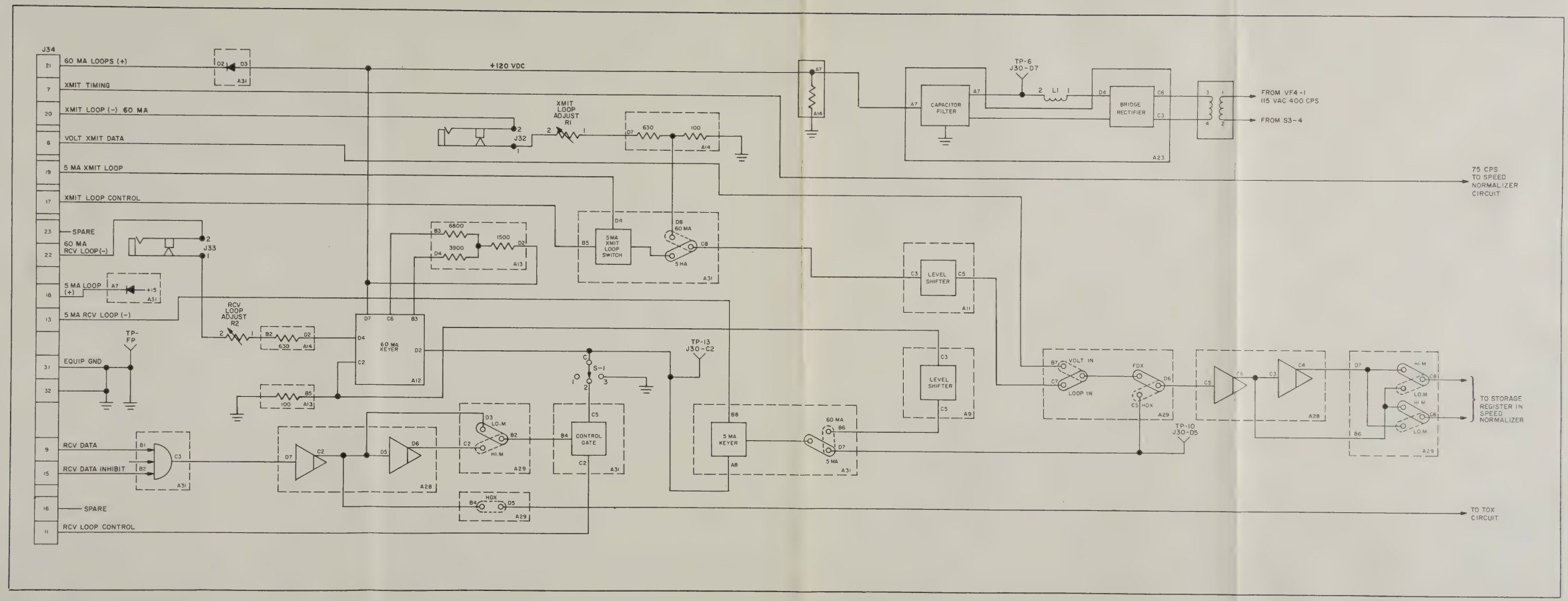


Figure 7-1. Receive and Transmit Loop Interface

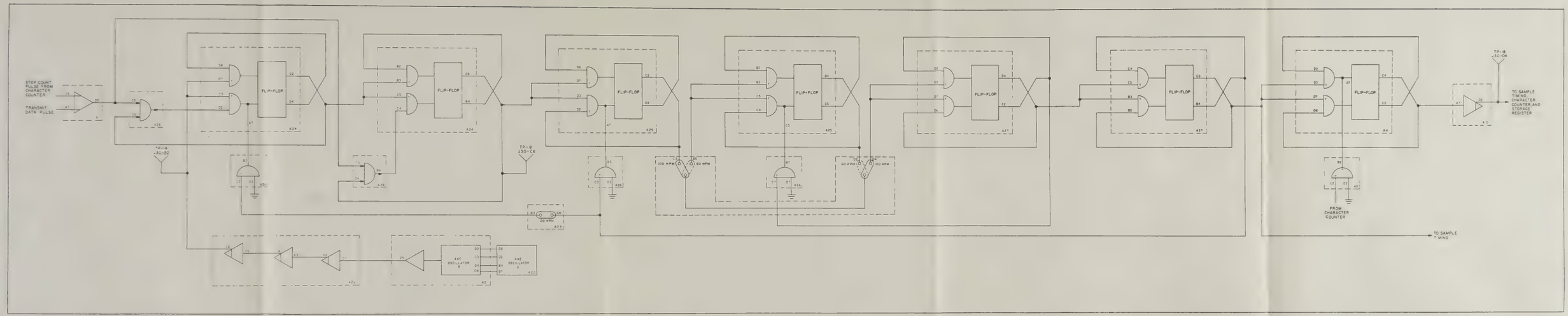


Figure 7-2. Bit Counter Logic Diagram.

Divider	3	2	1	Bit Count Pulse
	1	1	0	0
	1	0	1	1
	1	0	0	2
	0	1	1	3
	0	1	0	4
	0	0	1	5
	0	0	0	6
Feedback	1	1	1	7
Change Count	1	1	0	7

Figure 7-7. Table of Character Counter Logic States

7-31. The transmit data bits are gated and applied to the pedestal gates of the first register. The output pulses of the bit counter trigger the data into the register. The output of the first register enables the second register pedestal gates. The output pulses of the sample timing circuit triggers the data into the second register. The output of the second register enables the pedestal gates of the third register. The data is triggered into the third register by the external transmit timing 75 cps pulses. The logic one set output of the third register is fed through a control gate, an inversion circuit for proper data format and through an isolation gate to the transmission equipment. If two units are used, the isolation diode in the output circuit of one unit is combined with the diode of the second unit to comprise an AND gate circuit. The diode of the unit not being used is fed a constant logic one state (0 volts dc). The data output from the unit being used is gated out in synchronism with the logic one data bits applied to its isolation diode, and thereby through the enabled gate.

7-32. TOX (TELETYPE-OPERATE-TRANSMIT) CIRCUIT

7-33. A TOX (teletype-operate-transmit) circuit (figure 7-11)is incorporated in the 399R-1 Teletype Adapter. The TOX circuit is a teletype net-in-use monitor and automatic transmitter keying device used in half-duplex operation. The gated and inverted (figure 7-39) negative going edge of a Baudot character start bit in the teletype transmit data causes the memory circuit capacitor (figure 7-38) to change. The charged capacitor turns on the transistorized switch (figure 7-37). Turning on the switch causes the relay to activate, thereby causing a -15 volt level to be available for use in external equipment and closes the key-line to key a transmitter. The transmitter can be keyed, providing the KEYLINE switch S2 is closed.

7-34. When the teletype trans
ory circuit capacitor begins to
approximate six-second durati
charge, the relay is deactivate
receive level line and breakin

7-35. During half-duplex rec
unit is disabled by two means.
squelch signal disables the TC
data passing the inhibit gate ar
is also applied to the TOX dat
the gate is disabled by logic ze
circuit.

7-36. When the unit is neith
mitting, spurious noise that
may be on the receive data lir
is fed through the receive data
cuit to the TOX data inhibit ga
gate is disabled and the data is
the TOX circuit.

7-37. 399R-1 POWER SUPPI

7-38. The 399R-1 Teletype A
ure 7-12) converts 115 volts
volts, -15 volts, + 6 volts, and
power supply consists of an in
cuit, voltage regulator circu
cuits, filter circuits and an o
switch circuit permits the 39
be used either by an external
INTERNAL circuits.

7-39. INPUT CIRCUIT. The
PWR switch S1, fuse F1, and
The 115 volts, 400 cps input p
the PWR switch and fuse to
The center-tapped power tra
volts ac input to approximatel
each secondary and applies it

7-40. RECTIFIER CIRCUIT.
(figure 7-31) converts the inc
from the transformer to approx
The rectifier voltage is applie
lator circuit and -15 volts reg

7-41. VOLTAGE REGULATO
voltage regulator circuits (fi
identical function. Their pur
+15 volts and -15 volts power
in each regulator permits ma
voltage amplitude. The voltag
tects any changes to the adjust
sponse to the detected change
are applied through the ampli
to the series regulator. The se
in turn, by regulating the amo
load to compensate for any in
voltage. In the event of an exc
short circuit, the short circui
a signal through the amplifier
cut off the transistor in the s
This is accomplished by apply
base of the transistor.

7-42. VOLTAGE DIVIDER CI
voltage divider circuits are loc

Divider	3	2	1	Bit Count Pulse
	1	1	0	0
	1	0	1	1
	1	0	0	2
	0	1	1	3
	0	1	0	4
	0	0	1	5
	0	0	0	6
Feedback	1	1	1	7
Change Count	1	1	0	7

Figure 7-7. Table of Character Counter Logic States

7-31. The transmit data bits are gated and applied to the pedestal gates of the first register. The output pulses of the bit counter trigger the data into the register. The output of the first register enables the second register pedestal gates. The output pulses of the sample timing circuit triggers the data into the second register. The output of the second register enables the pedestal gates of the third register. The data is triggered into the third register by the external transmit timing 75 cps pulses. The logic one set output of the third register is fed through a control gate, an inversion circuit for proper data format and through an isolation gate to the transmission equipment. If two units are used, the isolation diode in the output circuit of one unit is combined with the diode of the second unit to comprise an AND gate circuit. The diode of the unit not being used is fed a constant logic one state (0 volts dc). The data output from the unit being used is gated out in synchronism with the logic one data bits applied to its isolation diode, and thereby through the enabled gate.

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7-34. When the teletype transmit data stops, the memory circuit capacitor begins to slowly discharge for an approximate six-second duration. At the end of the discharge, the relay is deactivated, thereby grounding the receive level line and breaking the keyline continuity.

7-35. During half-duplex receive operation, the TOX unit is disabled by two means. Normally a logic zero squelch signal disables the TOX inhibit gate. Receive data passing the inhibit gate and first inversion circuit is also applied to the TOX data input gate. However, the gate is disabled by logic zero signal from the keyer circuit.

7-36. When the unit is neither receiving or transmitting, spurious noise that simulates teletype data may be on the receive data line. This logic one noise is fed through the receive data gate and inversion circuit to the TOX data inhibit gate as a logic zero. The gate is disabled and the data is deterred from activating the TOX circuit.

7-37. 399R-1 POWER SUPPLY.

7-38. The 399R-1 Teletype Adapter power supply (figure 7-12) converts 115 volts, 400 cps power to +15 volts, -15 volts, + 6 volts, and -6 volts dc power. The power supply consists of an input circuit, rectifier circuit, voltage regulator circuits, voltage divider circuits, filter circuits and an output circuit. The output switch circuit permits the 399R-1 power supply to be used either by an external device or by the 399R-1 INTERNAL circuits.

7-39. INPUT CIRCUIT. The input circuit contains PWR switch S1, fuse F1, and power transformer T2. The 115 volts, 400 cps input power is applied through the PWR switch and fuse to the power transformer. The center-tapped power transformer converts 115 volts ac input to approximately 58 volts ac output on each secondary and applies it to the rectifier circuit.

7-40. RECTIFIER CIRCUIT. The rectifier circuit (figure 7-31) converts the incoming 58 volts ac power from the transformer to approximately ±25 VDC power. The rectifier voltage is applied to the +15 volts regulator circuit and -15 volts regulator circuit.

7-41. VOLTAGE REGULATOR CIRCUITS. The two voltage regulator circuits (figure 7-23) perform an identical function. Their purpose is to regulate the +15 volts and -15 volts power. A level adjust circuit in each regulator permits manual adjustment of the voltage amplitude. The voltage reference circuit detects any changes to the adjusted voltage level. In response to the detected changes, compensating signals are applied through the amplifier and regulator drive to the series regulator. The series regulator responds, in turn, by regulating the amount of current into the load to compensate for any increase or decrease in voltage. In the event of an excessive current drain or short circuit, the short circuit feedback circuit sends a signal through the amplifier and regulator drive to cut off the transistor in the series regulator circuit. This is accomplished by applying reverse bias to the base of the transistor.

7-42. VOLTAGE DIVIDER CIRCUITS. Two identical voltage divider circuits are located in the +15 volts and

-15 volts power circuits. These +6 volt and -6 volt dividers consist of a resistor and a Zener diode in series across the output. The +6 volts and -6 volts outputs are clamped at their respective amplitudes by the Zener diodes.

7-43. FILTER CIRCUITS. The filter circuits (figure 7-20) are used to eliminate the ripple voltages in the d-c power.

7-44. 120 VOLT POWER SUPPLY.

7-45. The input to the main power supply is also fed to the 120 volt power supply. This power supply consists of a power transformer, bridge rectifier circuit (figure 7-36), and a filter section. The 115 volts AC input to the power transformer is stepped up to 135 volts ac. The AC voltage is applied to a bridge rectifier and filtered to 120 volts DC for use in the 60 ma receive and transmit loop.

7-46. TROUBLE ANALYSIS.

7-47. The trouble analysis procedure for the 399R-1 consists of a general checkout procedure and a set of procedural tables. The general checkout procedure presupposes that the unit has been removed from a system installation for faulty operation. It further presupposes that the cause of the unit malfunction is unknown. For this reason, follow the general checkout procedure to isolate the trouble to a functional area. When the faulty functional area is located, the general checkout procedure refers to the applicable trouble analysis table.

7-48. The trouble analysis tables provide procedural steps to isolate the malfunction to a particular circuit card. When the faulty card is isolated, replacement is recommended. A schematic diagram of each circuit card in the unit, as well as an illustration giving card locations within the unit, is provided as an aid to locating the malfunction within a card. Also included are a table of logic symbols (figure 7-13) and a table of applicable waveforms (figure 7-14). Test point locations are indicated on figure 7-42. A cross reference of circuit card locations, assembly numbers, and schematic figure numbers is shown in figure 7-19.

7-49. Some procedural steps within the individual trouble analysis tables recommend repeating the general checkout procedure. It is strongly recommended that the general checkout procedure be repeated after the malfunction has been repaired. This assures that the unit is returned to a trouble free operating condition.

7-50. GENERAL CHECKOUT.

a. Power Supply Checkout.

1. Apply 115 volts ac, 400 cps power at pins J34-24 and J34-25.

2. Perform checks in figure 7-15 to checkout the power supply circuitry.

b. Test Setup

1. Remove 115 volts ac, 400 cps power from pins J34-24 and J34-25.

2. Change the XMIT strap on circuit card A31 to 60 ma.

3. Change the Strap circuit card A29 as follows:

XMIT DATA at LOOP IN

OPERATION at FDX

SPEED NORM INPUT at MARK

XMIT DATA RATE at 100 WPM

KEYER IN at LO MARK

4. Connect a teletype keyboard between J34-21 and J34-20.

5. Connect a teletype printer between J34-21 and J34-22.

6. Connect a jumper between J34-9 and J34-10.

7. Connect a jumper between J34-13 and J34-18.

8. Apply grounds at J34-11 and J34-12.

9. Apply 115 volts ac, 400 cps power at pins J34-24 and J34-25.

10. Adjust loop currents at 60 ma.

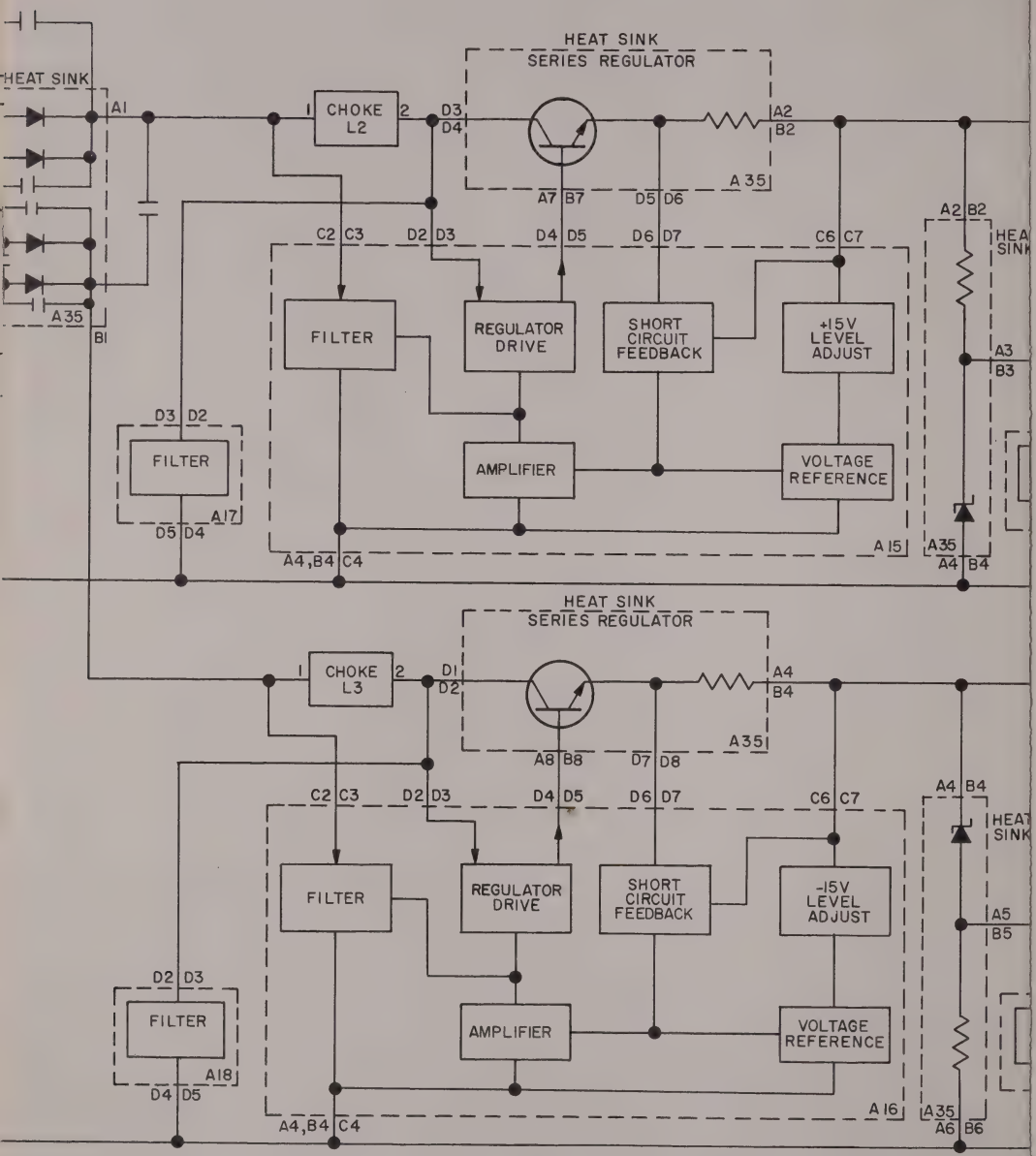
11. Set the KEYER INPUT switch (S1) at RCV DATA.

12. Apply 75 cps, 0/-6 volts dc square wave at J34-7.

c. Tests.

1. Type on the teletype keyboard. The typed information should appear on the printer copy. If the copy is the same as typed, proceed to figure 7-16. If the copy is garbled or no copy appears, proceed to step 2.

2. Connect an oscilloscope at J34-10, and continue to type. Observe 0/-6 volts dc pulses of 13.3 millisecond duration or integral multiples of 13.3 on the oscilloscope. If the square wave pulses are observed, proceed to figure 7-18. If the pulses are not observed proceed to figure 7-17.


HEAT SINK
SERIES REGULATOR
HEAT SINK
A1
B1
A35
CHOKE
L2
1
2
D3
D4
A2
B2
A7 B7
D5 D6
A35
C2 C3
D2 D3
D4 D5
D6 D7
C6 C7
FILTER
REGULATOR
DRIVE
SHORT
CIRCUIT
FEEDBACK
+15V
LEVEL
ADJUST
A3
B3
D3 D2
FILTER
A17
D5 D4
AMPLIFIER
VOLTAGE
REFERENCE
A15
A4,B4 C4
A2 B2
A35
A4 B4
HEAT SINK
SERIES REGULATOR
CHOKE
L3
1
2
D1
D2
A4
B4
A35
A8 B8
D7 D8
C2 C3
D2 D3
D4 D5
D6 D7
C6 C7
FILTER
REGULATOR
DRIVE
SHORT
CIRCUIT
FEEDBACK
-15V
LEVEL
ADJUST
A5
B5
D2 D3
FILTER
A18
D4 D5
AMPLIFIER
VOLTAGE
REFERENCE
A16
A4,B4 C4
A4 B4
A35
A6 B6

CARD LOC.	CARD NAME	ASSEMBLY NUMBER	SCHEMATIC (FIGURE) NUMBER
A 1	TELETYPE OPERATED TRANSMIT NO.3	8984	7 - 39
A 2	TELETYPE OPERATED TRANSMIT NO.2	8980	7 - 38
A 3	TELETYPE OPERATED TRANSMIT NO.1	8976	7 - 37
A 4	FLIP-FLOP	8964	7 - 35
A 5	LOGIC NO. 1A	9040	7 - 24
A 6	FLIP-FLOP	8964	7 - 35
A 7	FLIP-FLOP	8964	7 - 35
A 8	FLIP-FLOP	8964	7 - 35
A 9	LOGIC 2	9044	7 - 25
A10	INVERTER B	9000	7 - 22
A11	LOGIC 3	9048	7 - 26
A12	KEYER	8956	7 - 34
A13	RESISTOR 2	9192	7 - 33
A14	RESISTOR 1	9187	7 - 32
A15	POWER SUPPLY REGULATOR	9004	7 - 23
A16	POWER SUPPLY REGULATOR	9004	7 - 23
A17	POWER SUPPLY CAPACITOR	8992	7 - 20
A18	POWER SUPPLY CAPACITOR	8992	7 - 20
A19	SWITCH	5067	7 - 41
A20	4 KC OSCILLATOR A	9064	7 - 27
A21	4 KC OSCILLATOR B	9068	7 - 28
A22	INVERTER A	8996	7 - 21
A23	120 VOLT POWER SUPPLY	8972	7 - 36
A24	FLIP-FLOP	8964	7 - 35
A25	FLIP-FLOP	8964	7 - 35
A26	LOGIC NO. 1A	9040	7 - 24
A27	FLIP-FLOP	8964	7 - 35
A28	INVERTER A	8996	7 - 21
A29	STRAP	9108	7 - 29
A30	TEST POINTS	9121	7 - 30
A31	5 MA LOOP CONTROL	5061	7 - 40
A35	HEAT SINK	9205	7 - 31

Figure 7-19. Circuit Cards

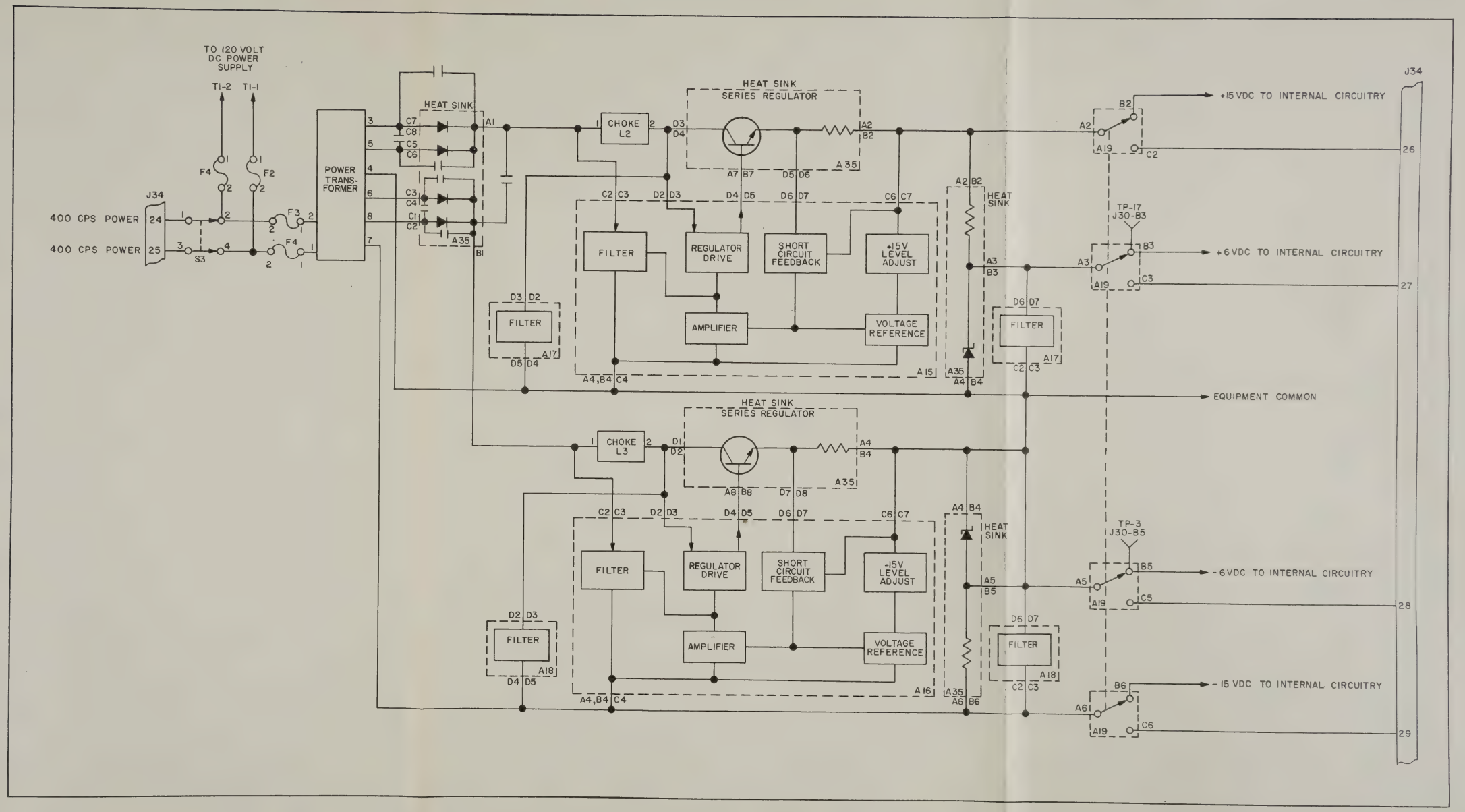


Figure 7-12. Power Supply Block Diagram

CARD LOC.	CARD NAME	ASSEMBLY NUMBER	SCHEMATIC (FIGURE) NUMBER
A 1	TELETYPE OPERATED TRANSMIT NO.3	8984	7 - 39
A 2	TELETYPE OPERATED TRANSMIT NO.2	8980	7 - 38
A 3	TELETYPE OPERATED TRANSMIT NO.1	8976	7 - 37
A 4	FLIP-FLOP	8964	7 - 35
A 5	LOGIC NO. 1A	9040	7 - 24
A 6	FLIP-FLOP	8964	7 - 35
A 7	FLIP-FLOP	8964	7 - 35
A 8	FLIP-FLOP	8964	7 - 35
A 9	LOGIC 2	9044	7 - 25
A10	INVERTER B	9000	7 - 22
A11	LOGIC 3	9048	7 - 26
A12	KEYER	8956	7 - 34
A13	RESISTOR 2	9192	7 - 33
A14	RESISTOR 1	9187	7 - 32
A15	POWER SUPPLY REGULATOR	9004	7 - 23
A16	POWER SUPPLY REGULATOR	9004	7 - 23
A17	POWER SUPPLY CAPACITOR	8992	7 - 20
A18	POWER SUPPLY CAPACITOR	8992	7 - 20
A19	SWITCH	5067	7 - 41
A20	4 KC OSCILLATOR A	9064	7 - 27
A21	4 KC OSCILLATOR B	9068	7 - 28
A22	INVERTER A	8996	7 - 21
A23	120 VOLT POWER SUPPLY	8972	7 - 36
A24	FLIP-FLOP	8964	7 - 35
A25	FLIP-FLOP	8964	7 - 35
A26	LOGIC NO. 1A	9040	7 - 24
A27	FLIP-FLOP	8964	7 - 35
A28	INVERTER A	8996	7 - 21
A29	STRAP	9108	7 - 29
A30	TEST POINTS	9121	7 - 30
A31	5 MA LOOP CONTROL	5061	7 - 40
A35	HEAT SINK	9205	7 - 31

Figure 7-19. Circuit Cards

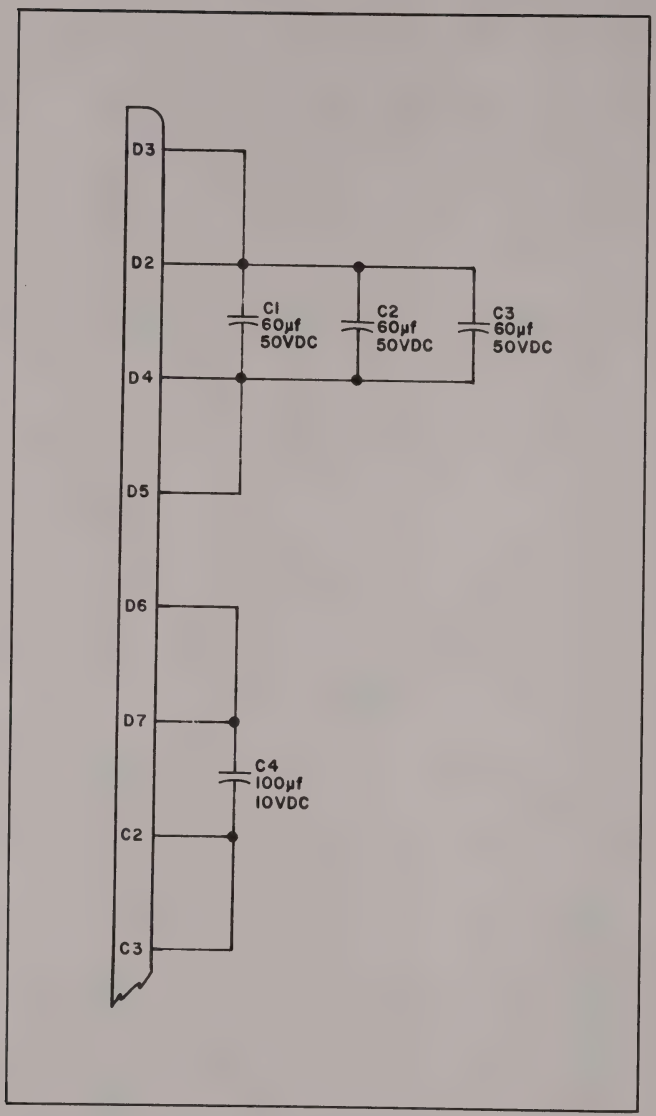


Figure 7-20. Power Supply Capacitors Schematic Diagram

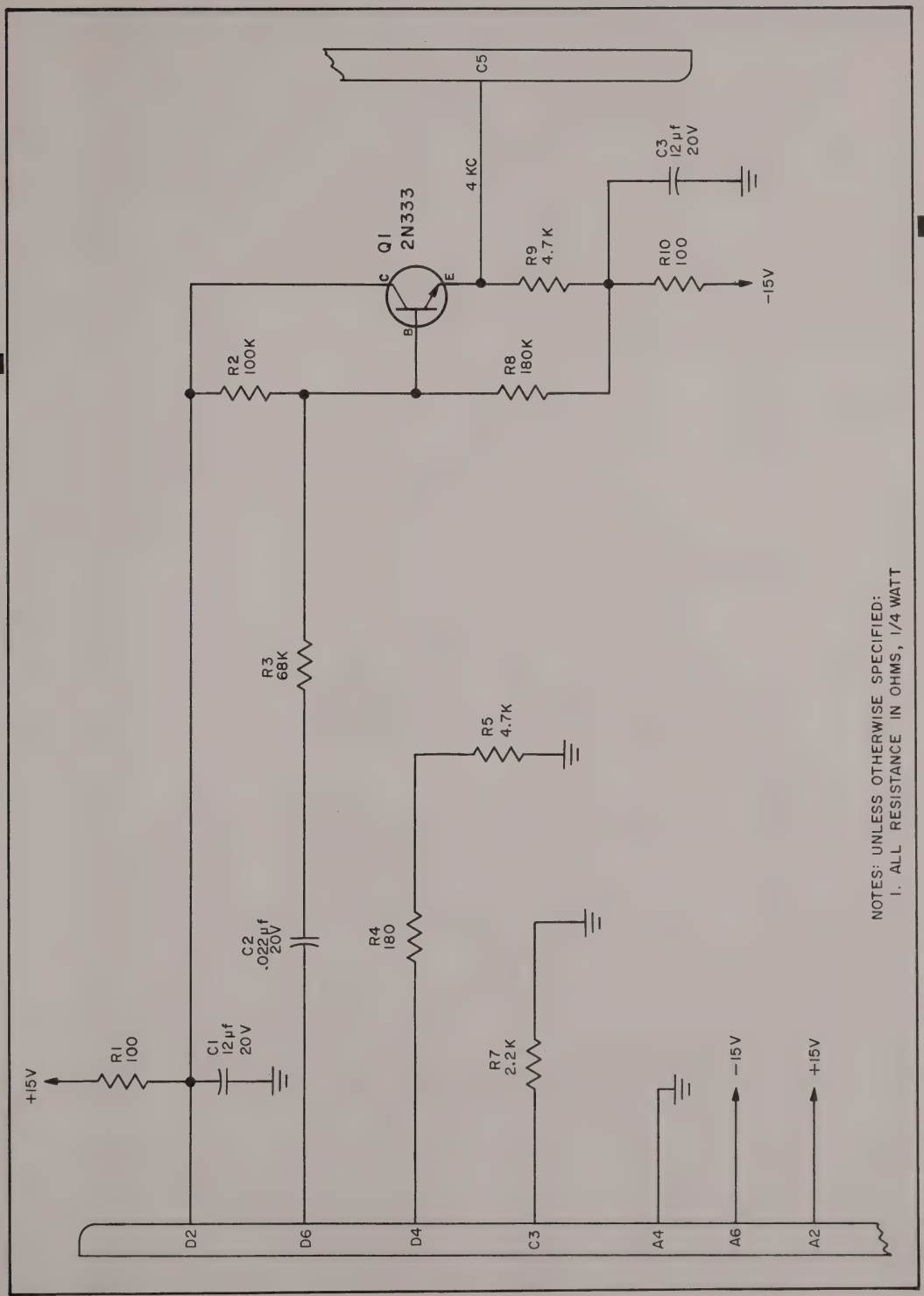


Figure 7-28. 4 KC Oscillator B, Schematic Diagram

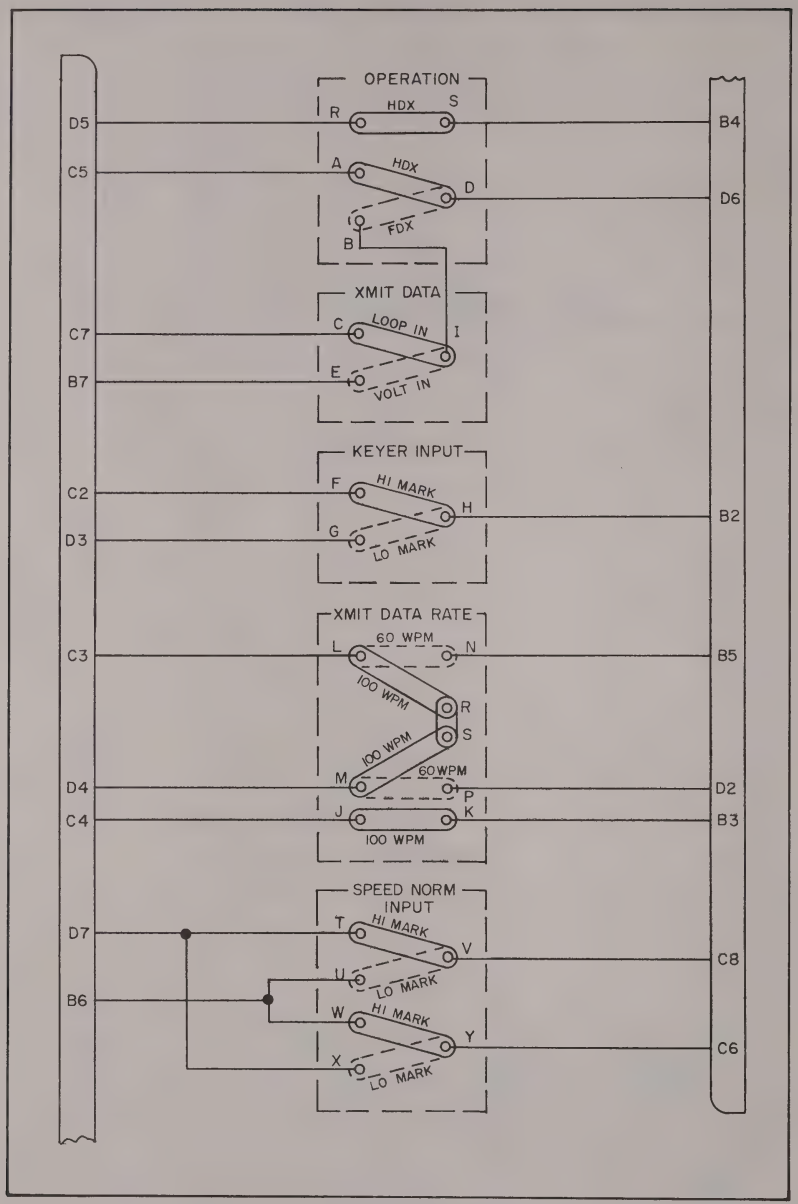


Figure 7-29. Strap, Schematic Diagram

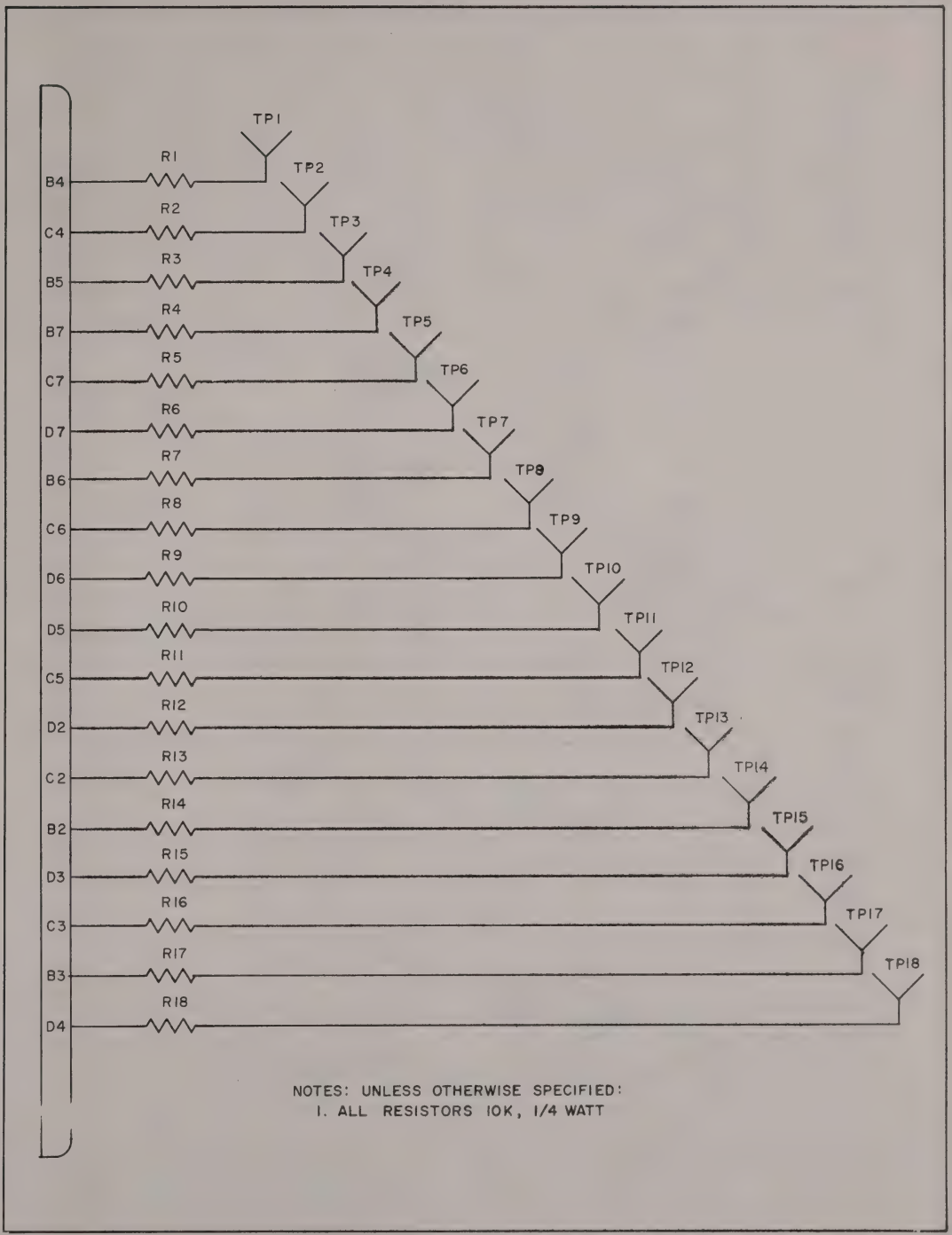


Figure 7-30. Test Points, Schematic Diagram

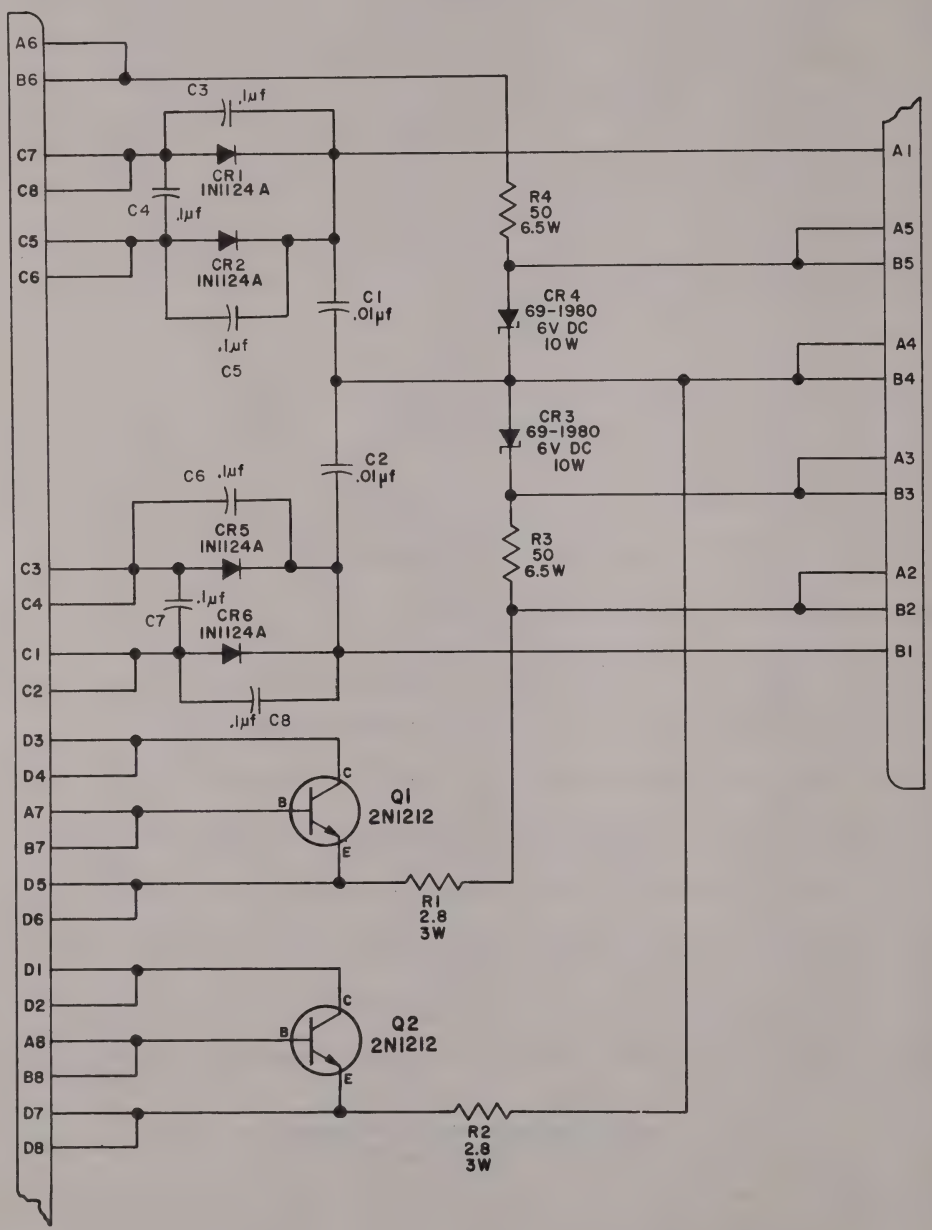


Figure 7-31. Heat Sink, Schematic Diagram

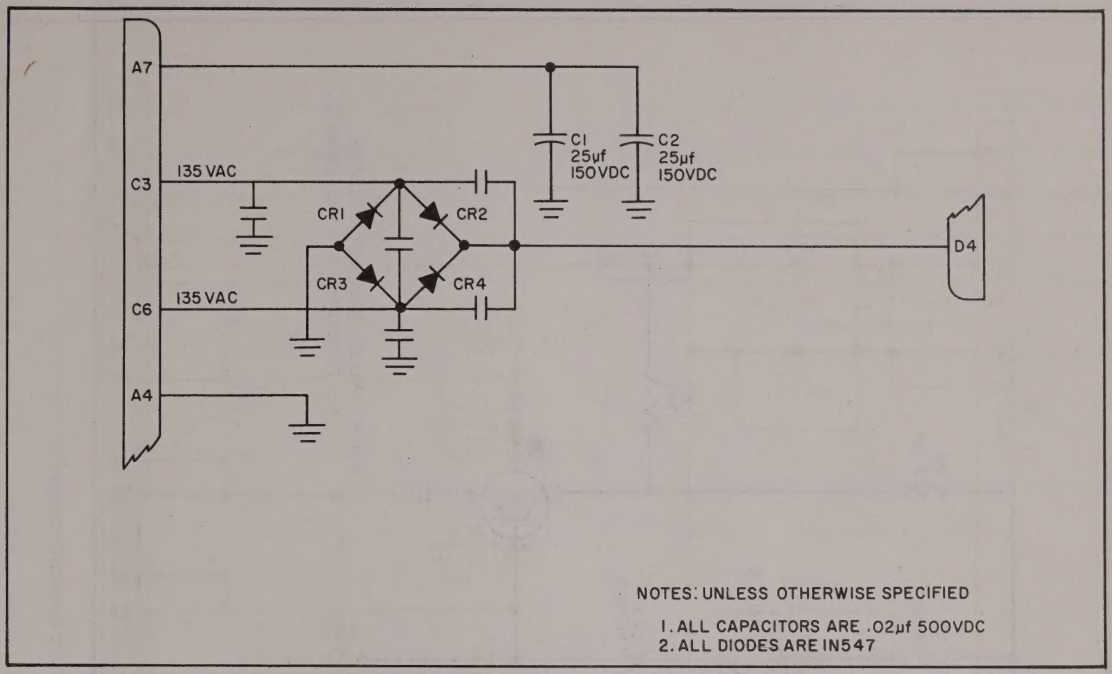


Figure 7-36. 120 Volt Power Supply, Schematic Diagram

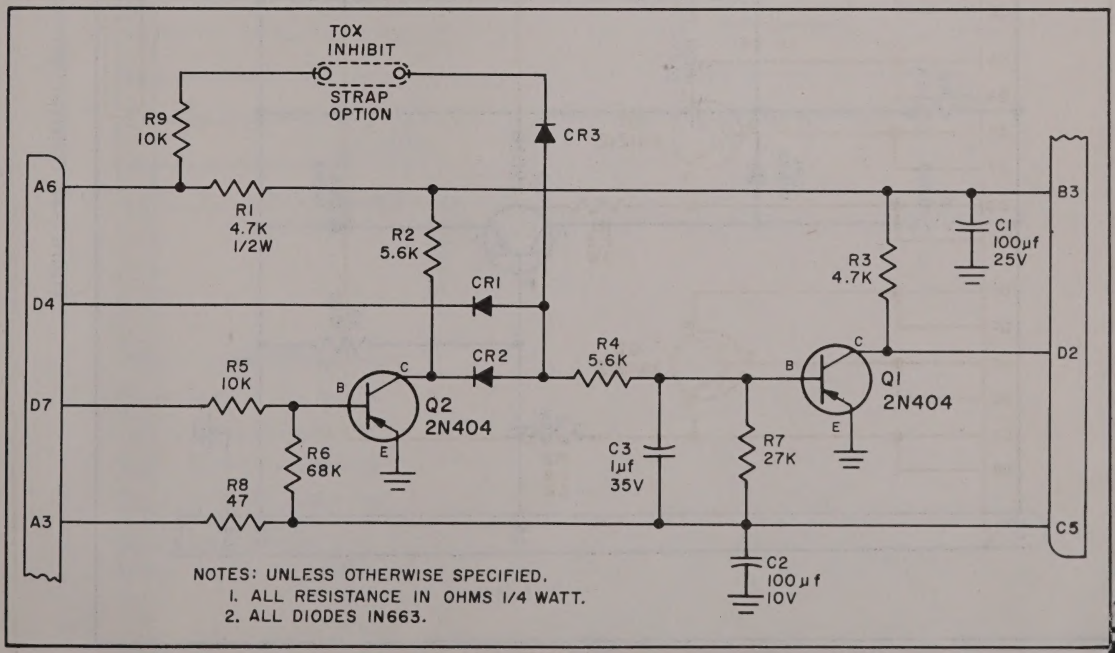


Figure 7-37. Teletype Operated Transmit No. 1 Schematic Diagram

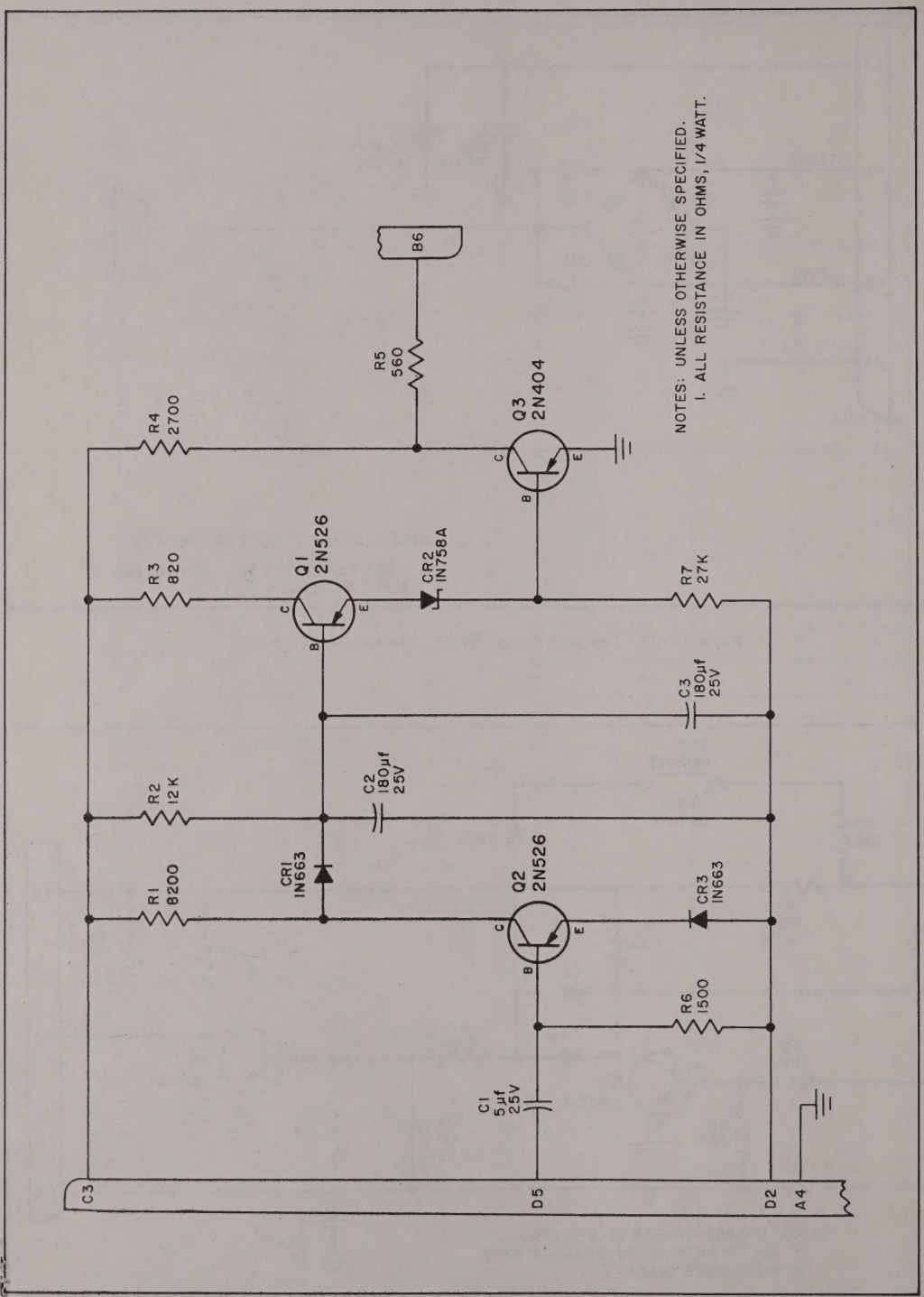
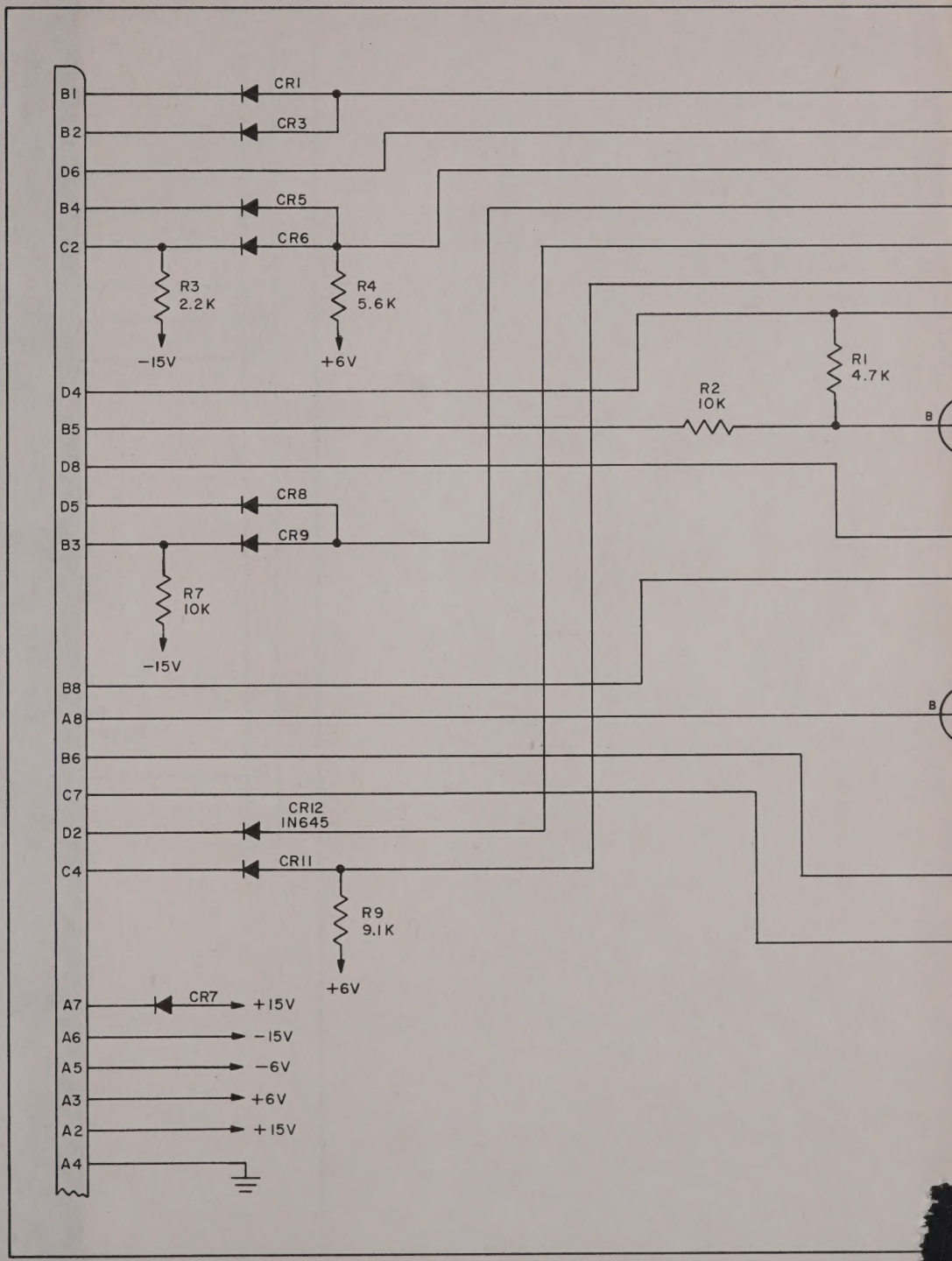
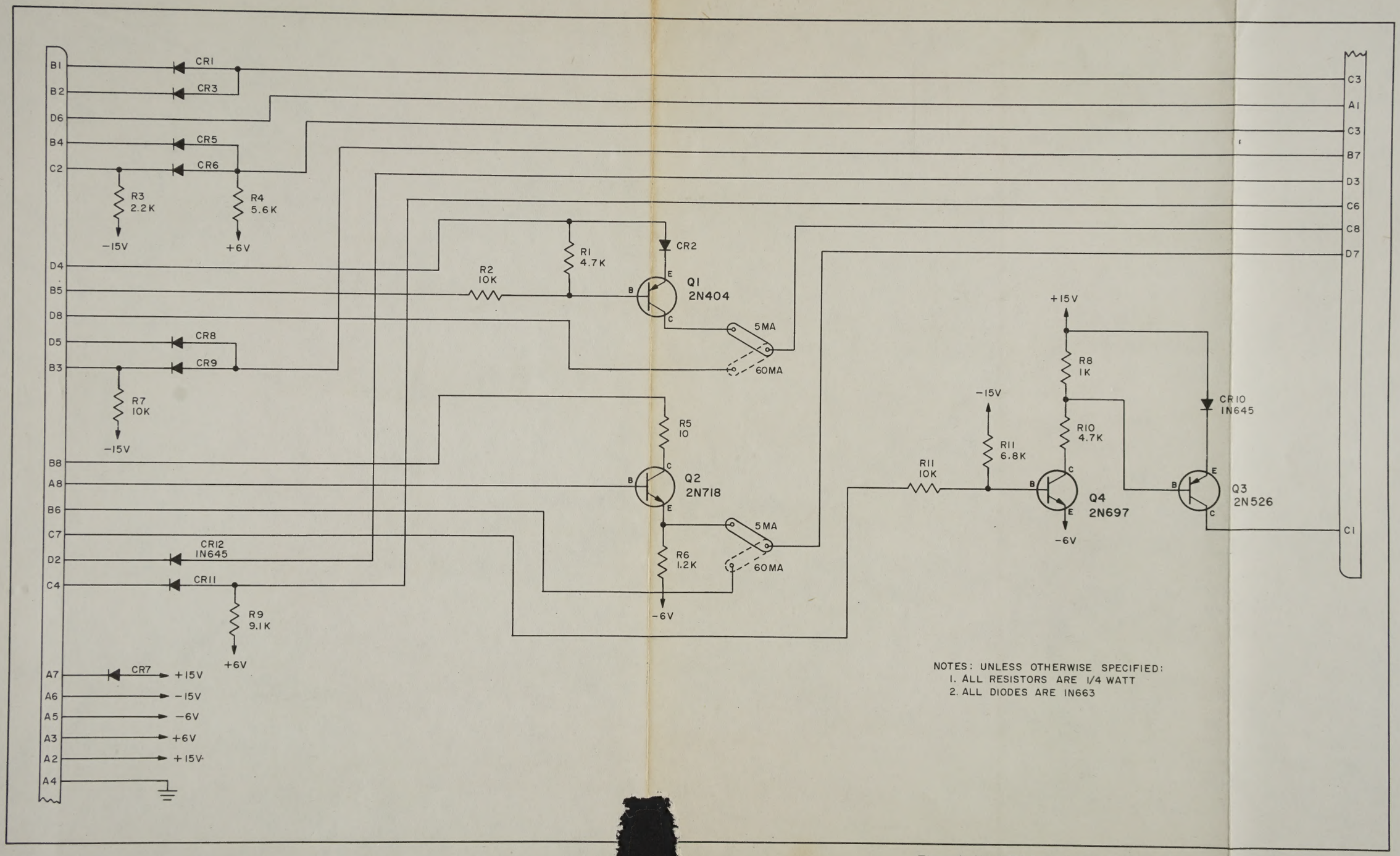


Figure 7-38. Teletype Operated Transmit No. 2 Schematic Diagram


B1
B2
D6
B4
C2
D4
B5
D8
D5
B3
B8
A8
B6
C7
D2
C4
A7
A6
A5
A3
A2
A4
CR1
CR3
CR5
CR6
CR8
CR9
CR12
IN645
CR11
CR7
R3
2.2K
R4
5.6K
R1
4.7K
R2
10K
R7
10K
R9
9.1K
−15V
+6V
−15V
+6V
+15V
−15V
−6V
+6V
+15V
B
B



NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/4 WATT
2. ALL DIODES ARE IN663

Figure 7-40. 5 MA Loop Control, Schematic Diagram